Amendments to the Specification

Page 1, line 7, please insert the following paragraph:

This application is a divisional of Application No. 09/931,915 filed August 20, 2001, incorporated herein by reference in its entirety.

Please replace the paragraph at page 1, line 24 to page 2, line 3, with the following paragraph:

An objective of the present invention is to provide: a memory cell array which is capable of decreasing the ~~parasitic capacitance~~ parasitic capacitance or load capacitance of signal electrodes and has ferroelectric layers making up ferroelectric capacitors and having a predetermined pattern; a method of fabricating the same; and a ferroelectric memory device including the memory cell array of the present invention.

Please replace the paragraphs at page 2, line 21 to Page 4, line 14, with the following paragraphs:

In this memory cell array, since the ferroelectric layer is formed linearly along one of the first and second signal electrode, the ~~parasitic capacitance~~ parasitic capacitance or load capacitance of the other of the first and second signal electrodes can be decreased.

According to a second aspect of the present invention, there is provided a second memory cell array having ferroelectric capacitors, wherein: memory cells formed of ferroelectric capacitors are arranged in a matrix; each of the ferroelectric capacitors includes a first signal electrode, a second signal electrode disposed in a direction intersecting the first signal electrode, and a ferroelectric layer disposed at least in an intersection area of the first and second signal electrodes; and the ferroelectric layer is disposed only in the intersection area of the first and second signal electrodes. In this memory cell array, since the

ferroelectric layers making up the ferroelectric capacitors are formed in the smallest region, the ~~parasitic capacitance~~ parasitic capacitance or load capacitance of the signal electrodes can be further decreased.

In this memory cell array, since the ferroelectric layer forming the ferroelectric capacitor has a minimum area, the ~~parasitic capacitance~~ parasitic capacitance or load capacitance of the signal electrodes can be further reduced.

The above memory cell arrays have the following features.

(A) The ferroelectric capacitors may be disposed on a base; and a dielectric layer may be provided between laminates each of which includes the first signal electrode and the ferroelectric layer so as to cover an exposed surface of the base. In this case, the dielectric layer may be formed of a material having a dielectric constant lower than a dielectric constant of the ferroelectric layer. The ~~parasitic capacitance~~ parasitic capacitance or load capacitance of the signal electrodes can be reduced effectively by providing such dielectric layer.

(B) An undercoat layer having surface properties differing from surface properties of the base may be formed on the base. By providing such undercoat layer, at least either the signal electrode or the ferroelectric layer can be formed selectively without etching. The undercoat layer may be provided in an area in which the ferroelectric capacitors are not formed; and a surface of the undercoat layer may have a low affinity for a material forming the ferroelectric capacitors, in comparison with a surface of the base. Alternatively, the undercoat layer may be provided in an area in which the ferroelectric capacitors are formed; and a surface of the undercoat layer may have a high affinity for a material forming the ferroelectric capacitors, in comparison with a surface of the base.

Please replace the paragraph at page 11, lines 6-22, with the following paragraph:

Dielectric layers 18 are formed between laminates consisting of the ferroelectric layer 14 and the second signal electrode 16 so as to cover exposed areas of the base 10 and the first signal electrodes 12. The dielectric layers 18 preferably have a dielectric constant lower than that of the ferroelectric layers 14. The ~~parasitic capacitance~~ parasitic capacitance or load capacitance of the second signal electrodes 16 can be decreased by allowing the dielectric layers 18 having a dielectric constant lower than that of the ferroelectric layers 14 to be interposed between the laminates consisting of the ferroelectric layer 14 and the second signal electrode 16. As a result, a read or write operation of the ferroelectric memory device 1000 can be performed at a higher speed.

In this embodiment, the ferroelectric layers 14 are formed linearly along the second signal electrodes 16. The ~~parasitic capacitance~~ parasitic capacitance or load capacitance of the first signal electrodes 12 can be decreased by forming the ferroelectric layers 14 linearly.

Please replace the paragraph at page 18, lines 1-13, with the following paragraph:

The ferroelectric layers 14 are selectively formed on the first signal electrodes 12. Undercoat layers 22 are formed on the base 10 between the first signal electrodes 12. The dielectric layers 18 are formed on the undercoat layers 22. The dielectric layers 18 preferably have a dielectric constant lower than that of the ferroelectric layers 14. The ~~parasitic capacitance~~ parasitic capacitance or load capacitance of the second signal electrodes 16 can be decreased by allowing the dielectric layers 18 having a dielectric constant lower than that of the ferroelectric layers 14 to be interposed between laminates consisting of the first signal electrode 12 and the ferroelectric layer 14. As a result, a read or write operation of the ferroelectric memory device can be performed at a higher speed.

Please replace the paragraphs at page 30, line 21 to page 31, line 12, with the following paragraphs:

The dielectric layers 18 and the dielectric layers which are optionally formed preferably have a dielectric constant lower than that of the ferroelectric layers 14. The ~~parasitic capacitance~~ parasitic capacitance or load capacitance of the first signal electrodes 12 and the second signal electrodes 16 can be decreased by allowing the dielectric layers having a dielectric constant lower than that of the ferroelectric layers 14 to be interposed between the laminates consisting of the first signal electrode 12 and the ferroelectric layer 14 or between the laminates consisting of the ferroelectric layer 14 and the second signal electrode 16. As a result, a read or write operation of the ferroelectric memory device can be performed at a higher speed.

In this embodiment of the present invention, the ferroelectric layers 14 which make up the ferroelectric capacitors 20 are formed only in the intersection regions between the first signal electrodes 12 and the second signal electrodes 16. According to this configuration, the ~~parasitic capacitance~~ parasitic capacitance or load capacitance of both the first signal electrodes 12 and the second signal electrodes 16 can be decreased.

Please add the following new paragraph at page 9, line 16, after the fifth full paragraph:

Fig. 25 is a cross-sectional view schematically showing a step of the method of fabricating a memory cell array according to an exemplary embodiment of the invention.

Please replace the paragraph at page 27, lines 3-16 with the following paragraph:

In this embodiment, the undercoat layers 22 are formed in the second regions 26 so that the first regions 24 and the second regions 26 have surface properties differing in